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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,281	01/30/2004	Tae-Sung Kim	P57002	4288
7590 Robert E. Bushnell Suite 300 1522 K Street, N.W. Washington, DC 20005		03/09/2007	EXAMINER WARREN, MATTHEW E	
			ART UNIT 2815	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	03/09/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/767,281 Examiner Matthew E. Warren	KIM ET AL. Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,4-9,11-15,17-19 and 21-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,4-9,11-15,17-19 and 21-24 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>9/14/06, 9/25/06</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the Appeal Brief filed on November 22, 2006.

Response to Arguments

The Appeal Brief filed on November 22, 2006 is persuasive. The rejection of the previous Office Action is withdrawn but resubmitted to clarify the rejections of claims 8, 18, and 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 4-7, 9, 14, 15, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (US 6,271,543 B1) in view of Maeda (US 5,278,099).

In re claims 1 and 14, Ohtani shows (figs. 2A-3A and col. 6, line 38 – col. 7, line 22) a thin film transistor (208), comprising a source electrode (206), a drain electrode (207), a gate electrode (202) and a semiconductor layer (201), wherein one of the source electrode and the drain electrode comprises an aluminum layer disposed between a pair of titanium layers (col. 7, lines 10-13). Ohtani shows all of the elements of the claims except the aluminum layer being an aluminum alloy and a diffusion

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prevention layer interposed between the aluminum alloy layer and each of the pair of titanium layers. Maeda shows (fig. 1F) a source/drain electrode having a titanium layer (32), an aluminum alloy layer (36) (col. 4, lines 22-31), and a titanium nitride layer (34) interposed between the Ti and Al alloy to act as a barrier for blocking Al diffusion and preventing the growth of alloy spikes (col. 3, lines 46-61). The aluminum layer may be alloyed with Si to reduce the resistance and prevent openings in the wiring (col. 4, lines 22-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ti/Al/Ti source/drain electrode of Ohtani by alloying Si with aluminum and forming TiN between the Ti and Al alloy layers as taught by Maeda to reduce resistance of the contact and prevent Al diffusion and the growth of alloy spikes.

In re claims 2 and 15, Maeda discloses (col. 4, lines 22-31) that the aluminum alloy layer comprises an element selected from a group consisting of silicon, copper, neodymium, platinum and nickel. Maeda does not disclose the specific weight percentage of the element in the alloy. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the aluminum alloy having the desired percentage of an element, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 4 , Maeda discloses (col. 3, lines 46-61) each diffusion prevention layer is made of titanium nitride.

In re claims 5 and 6, the references do not teach the thickness of the titanium nitride or the percentage of nitrogen in the TiN being within the desired range. However, it would have been obvious to one of ordinary skill in the art to make the thickness of the TiN layer or the percentage of nitrogen within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233:

In re claims 7 and 19, Maeda discloses (col. 4, lines 22-31) that the Al electrode is an alloy containing Si and is therefore absent of pure aluminum.

In re claims 17 and 18, a "product by process" claim limitation is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 116 (*In re Wertheim*, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and *In re Marosi et al*, 218 USPQ 289 final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the

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prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

In re the remaining limitations of claim 18 concerning the conductive channel formed between the source and drain electrodes, Ohtani discloses (col. 6, lines 63-67) that a channel is formed between the source and drain of the device. The semiconductor is also primarily made of silicon (col. 6, lines 51-58) and contains the conductive channel.

Claims 8-13 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (US 6,271,543 B1) in view of Maeda (US 5,278,099) and Yamazaki et al. (US Pub. 2003/0222575 A1).

In re claims 8 and 21, Ohtani shows (figs. 2A-3A) a flat panel display and a process for making a flat panel display (col. 6, line 38 – col. 7, line 26) comprising forming: a substrate; a first plurality of thin film transistors formed on a surface of the substrate (there is a plurality of TFT's because the invention pertains to an active matrix array-which is known to contain many devices), the first plurality of thin film transistors comprising first source electrodes (connected 206), first drain electrodes (207), first gate electrodes (connected 202), and semiconductor layers (201); a plurality of first conductive lines (source wiring lines) electrically connected to the first source electrodes; and a plurality of second conductive lines (gate wiring lines) electrically connected to the first gate electrodes. Although Ohtani does not show the complete active matrix having a second plurality of thin film transistors, wherein the first drain

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electrodes of the first plurality of thin film transistors are electrically connected to gate electrodes of the second plurality of thin film transistors, such a recitation is of a well known routing scheme. For instance Yamazaki et al. discloses [0175] a complete device having the gate electrode of one TFT connected to a drain electrode of another TFT for a driving circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the routing scheme of Ohtani by adding a plurality of TFTs and connecting them as taught by Yamazaki to form a complete device having a driving circuit.

Furthermore, Ohtani discloses (col. 7, lines 10-13). that one of the first source electrodes, the first drain electrodes, the plurality of first conductive lines, and the plurality of second conductive lines comprises an aluminum layer disposed between a pair of titanium layers Ohtani shows all of the elements of the claims except the alloy layer being an aluminum alloy and a diffusion prevention layer interposed between the aluminum alloy layer and each of the pair of titanium layers. Maeda shows (fig. 1F) a source/drain electrode having a titanium layer (32), an aluminum alloy layer (36) (col. 4, lines 22-31), and a titanium nitride layer (34) interposed between the Ti and Al alloy to act as a barrier for blocking Al diffusion and preventing the growth of alloy spikes (col. 3, lines 46-61). The aluminum layer may be alloyed with Si to reduce the resistance and prevent openings in the wiring (col. 4, lines 22-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ti/Al/Ti source/drain electrode of Ohtani by alloying Si with aluminum and forming

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TiN between the Ti and Al alloy layers as taught by Maeda to reduce resistance of the contact and prevent Al diffusion and the growth of alloy spikes.

In re claims 9 and 22, Maeda discloses (col. 4, lines 22-31) that the aluminum alloy layer comprises an element selected from a group consisting of silicon, copper, neodymium, platinum and nickel. Maeda does not disclose the specific weight percentage of the element in the alloy. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the aluminum alloy having the desired percentage of an element, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claims 11 and 23, Maeda discloses (col. 3, lines 46-61) each diffusion prevention layer is made of titanium nitride.

In re claims 12, 13, and 24, the references do not teach the thickness of the titanium nitride or the percentage of nitrogen in the TiN being within the desired range. However, it would have been obvious to one of ordinary skill in the art to make the thickness of the TiN layer or the percentage of nitrogen within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Response to Arguments

Applicant's arguments filed with respect to claims 1, 2, 4-9, 11-15, 17-19, and 21-24 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the elements of the claims, specifically citing that Ohtani only discloses Ti/Al/Ti structure and does not disclose an aluminum alloy layer. The examiner believes that the prior art references show all of the elements of the claims and that the combined references show all of the elements of the claims. As stated in the rejection above, Ohtani discloses that the source and drain electrodes have a Ti/Al/Ti structure, but does not specifically disclose that the Al layer is an aluminum alloy layer. The gate electrode having the same Ti/Al/Ti structure is cited in Ohtani as using an Al alloy layer. Therefore, it is assumed that the source and drain electrodes of Ohtani may also comprise an Al alloy. However, Maeda was cited in part to cure the deficiencies of Ohtani in that respect and disclose that an electrode can comprise an alloy of aluminum. Maeda specifically disclosed in column 4, lines 22-31 that aluminum can be alloyed with Si to reduce the resistance of the layer. Therefore, Maeda cures the deficiencies of Ohtani and the combined references show all of the elements of the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571)

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272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren



March 5, 2007